CLAIMS

1. A semiconductor storage device comprising:

one or more memory planes in which a plurality of memory cells are arranged in a row direction and column direction in the form of an array and the memory cells in the same column are connected to a common bit line to form a memory block, and a plurality of the memory blocks are arranged in the column direction;

at least two global bit lines extending across the memory planes in the column direction each of which can be connected to one or more of the bit lines of each of the memory blocks through each bit line selection element; and

a block selection circuit, at the time of a reading operation, for selecting a selected memory block containing a selected memory cell to be read out by putting one of the bit line selection elements into a conduction state so that the bit line connected to the selected memory cell is connected to the one global bit line and for selecting a memory block other than the selected memory block as a dummy block by putting another one of the bit line selection elements into a conduction state so that one of the bit lines in the other memory block is connected to the other global bit line, wherein

when a defective block is contained in one or more of the memory planes, the block selection circuit generates a dummy block address for selecting the dummy block that is different from both of a selected block address of the selected memory block and a defective block address of the defective block by a predetermined logical operation targeted for a specific partial bit of each address bit of the selected block address .

2. A semiconductor storage device comprising:

one or more memory planes in which a plurality of memory cells are arranged in a row direction and column direction in the form of an array and the memory cells in the same column are connected to a common bit line to form a memory block, and a plurality of the memory blocks are arranged in the column direction;

at least two global bit lines extending across the memory planes in the column direction each of which can be connected to one or more of the bit lines of each of the memory blocks through each bit line selection element; and

a block selection circuit, at the time of a reading operation, for selecting a selected memory block containing a selected memory cell to be read out by putting one of the bit line selection elements into a conduction state so that the bit line connected to the selected memory cell is connected to the one global bit line and for selecting a memory block other than the selected memory block as a dummy block by putting another one of the bit line selection elements into a conduction state so that one of the bit lines in the other memory block is connected to the other global bit line, wherein

when a defective block is contained in the memory plane containing the selected memory block, the block selection circuit generates a dummy block address for selecting the dummy block that is different from both of a selected block address of the selected memory block and a defective block address of the defective block by a predetermined logical operation targeted for a specific partial bit of each address bit of the selected block address .

3. The semiconductor storage device according to claims 1 or 2, wherein the device is so constituted that, when one of the memory blocks in the memory plane is a defective block, the memory block can be repaired by replacing with a redundant block in block.

4. The semiconductor storage device according to claims 1 or 2, wherein the block selection circuit performs a first logical operation targeted for one or more of the specific partial bits of the selected block address to generate a dummy block address for selecting the dummy block, and when the dummy block address generated by the first logical operation coincides with the defective block address, performs a second logical operation targeted for another one or more of the specific partial bits of the selected block address to generate the dummy block address.

5. The semiconductor storage device according to claim 4, wherein coincidence between the dummy block address and the defective block address is determined by coincidence between the selected block address and the defective block address targeted for address bits except for one or more of the specific partial bits related to the first logical operation.

6. The semiconductor storage device according to claims 1 or 2, wherein the block selection circuit performs a first logical operation targeted for one or more predetermined bits of the specific partial bits of the selected block address, and performs a second logical operation targeted for one or

more bits except for the predetermined bits of the specific partial bits of the defective block address, to generate the dummy block address.

7. The semiconductor storage device according to claims 1 or 2, wherein a number of the partial bits is 2.

8. The semiconductor storage device according to claims 1 or 2, wherein the first and second logical operations are inverting operations of address bits.

9. The semiconductor storage device according to claims 1 or 2, wherein a plurality of memory blocks selected by combination of the specific partial bits of a block address to select the memory block are sequentially adjacent to each other to form a sub-memory plane.

10. The semiconductor storage device according to claims 1 or 2, further comprising a reference circuit and a differential input type of sensing circuit, wherein

the one global bit line connected to the bit line in the selected memory block is connected to one input of the sensing circuit directly or through a global bit line selection element, the other global bit line connected to the bit line in the dummy block is connected to the other input of the sensing circuit directly or through a global bit line selection element,

the reference circuit has a reference memory cell selectively connected to one of the inputs of the sensing circuit or one of the pair of

global bit lines, and

at the time of a reading operation, the reference memory cell is connected to the input of the sensing circuit for the dummy block.